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EXAMINER	
KAWSAR, ABDULLAH AL	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,150	SAMRA, NICHOLAS G.	
	Examiner	Art Unit	
	ABDULLAH AL KAWSAR	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/02/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following claim languages are not clearly understood and indefinite:

i. Claims 1-30, it is unclear how the elements of the invention are connected to each other. The relation between or the connectivity between active thread state, 1st and 2nd active thread, virtual state mechanism, virtual thread state, next thread multiplexer, virtual state reload multiplexer, state register and state restoration multiplexer.

ii. Claim 1, line 2 recites "first active thread" it is unclear if the system has only one thread or multiple thread (i.e. 2nd, 3rd or 4th thread? Multi-threaded?). Line 2 also recites " using a virtual state mechanism" it is unclear what is a virtual state mechanism and how does that define the active state of a thread (i.e. what are elements of virtual thread mechanism and operation?). Line 4 recites "generating virtual thread state" it is unclear where is it generated and who generates the virtual thread (i.e. generating in virtual sate mechanism? how?).

iii. Claims 9, 28 and 23 have similar deficiencies as claim 1 above.

iv. Claim 2, line 1 recites "active thread state" and "next thread multiplexer" it is unclear how the elements are connected or how the thread state is received from next thread multiplexer wherein claim 1 active thread state was received from virtual thread mechanism? (i.e. virtual thread mechanism is the next thread multiplexer?).

v. Claim 3, line1 recites "active thread state" and "virtual state reload multiplexer" it is unclear where is the virtual thread reload multiplexer located and the connection between active thread state, next thread multiplexer, first active thread and virtual thread mechanism.

vi. Claim 11 has similar deficiencies as claim 3 above.

vii. Claim 5, line 1 recites "reloading" it is unclear how the thread state is reloaded using the virtual reload multiplexer? (i.e. loop the output to input of virtual state mechanism?). line 1 also recites "every cycle" it is unclear what is meant by every cycle (i.e. different stage of update or every clock cycle?). line 3 recites "as long as" it is unclear what is defined by as long as or how to detect (i.e. thread switch? state change?).

viii. Claims 10, 5 and 24 have similar deficiencies as claim 5 above.

ix. Claim 6, line 2 recites "maintaining the virtual thread state" and "until the first active thread becomes active" it is unclear if the virtual thread state stays active or not after the first thread state is not active anymore (i.e. does the virtual thread state is replaced with the second thread or no more virtual thread state?).

Line 5 recites "detecting the activation" it is unclear how it is detected that a second thread is activated.

x. Claims 9, 17, 21, 28 and 25 have similar deficiencies as claim 6 above.

xi. Claim 7, line 5 recites "updating the virtual thread state" it is unclear if only one virtual thread state exist at once or more virtual thread states are available.

xii. Claims 14, 18, 22 and 26 have similar deficiencies as claim 7 above,

xiii. Claim 8, line 4 recites "detecting an uncommon event" it is unclear what is defined by an uncommon event? (i.e. cache miss or failure or stall or error condition?).

xiv. Claim 27 has similar deficiencies as claim 8 above.

xv. Claim 14, line 2 recites "detecting the activation" it is unclear how it is detected that a second thread is activated.

xvi. Claim 15, line 2 recites "first active thread" it is unclear if the system has only one thread or multiple thread (i.e. 2nd, 3rd or 4th thread? Multi-threaded?). Line 2 also recites "virtual state reload multiplexer to receive" it is unclear where the thread is being received and how the elements are connected. Line 4 recites "state register generate virtual thread state" it is unclear what is defined by a virtual thread state and how it is generated.

xvii. Claim 19 has similar deficiencies as claim 15 above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 5-7, 9-11, 13-26, 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flynn et al.(Flynn) US Patent No. 5907702, in view of Applicant Admitted Prior ART(AAPA).

6. As per claim 1, Flynn teaches the invention substantially as claimed including a method, comprising:

receiving active thread state using a virtual state mechanism (col 2, lines 57-64);

generating virtual thread state in accordance with the active thread state of the first active thread(col 4, lines 19-24); and

forwarding the virtual thread state corresponding to the first active thread to state update logic (figure 2, instruction dispatch from the output multiplexer 16).

Flynn does not specifically disclose receiving active thread state of the first active thread; forwarding the thread state to the state update logic.

However, AAPA teaches receiving active thread state of the first active thread and forwarding the thread state to the state update logic (page 3, par. 005, lines 4-7, specification).

7. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of AAPA into the method of Flynn to forward the thread state to the state update logic. The modification would have been obvious because one of the ordinary skills of the art would utilize that after the selection of the active thread the thread state will be forwarded to the state update logic as it is well known operation of the thread selection process in a multi-threaded system.

8. As per claim 2, Flynn teaches the active thread state is received from a next thread (NT) multiplexer (col 3, lines 40-42; figure 2, element 8).

9. As per claim 3, Flynn teaches the active thread state is received by a virtual state reload multiplexer of the virtual state mechanism (col 4, lines 13-18; figure 2, element 12).

10. As per claim 5, AAPA teaches for every cycle, reloading the virtual thread state corresponding to the first active thread using the multiplexer for as long as the first active thread remains active (par. 005, lines 9-16).

AAPA does not specifically disclose using a state reload multiplexer as long as the first thread remains active.

However, Flynn teaches using a state reload multiplexer as long as the first thread remains active (col 4, lines 13-18; figure 2, element 12).

11. As per claim 6, Flynn teaches maintaining the virtual thread state using the virtual thread mechanism until the first active thread becomes inactive and a second thread becomes active (col 4, lines 13-18; figure 2, element 16); and

detecting the activation of the second active thread (col 4, lines 19-24; lines 61-65).

12. As per claim 7, Flynn teaches receiving active thread state of the second active thread if the activation of the second active thread is detected(col 4, lines 13-18);

updating the virtual thread state in accordance with the active thread state of the second active thread (col 4, lines 61-65); and

forwarding the virtual thread state corresponding to the second active thread (figure 2, instruction dispatch from the output multiplexer 16).

Flynn does not specifically disclose forwarding the thread state to the state update logic.

However, AAPA teaches forwarding the thread state to the state update logic (page 3, par. 005, lines 4-7, specification).

13. As per claim 9, Flynn teaches the invention substantially as claimed including a method, comprising:

receiving active thread state using a virtual state mechanism(col 2, lines 57-64);

generating virtual thread state in accordance with the active thread state of the first active thread (col 4, lines 19-24); and

maintaining the virtual thread state corresponding to the first active thread until the first active thread becomes inactive(col 4, lines 13-18; figure 2, element 16).

However, AAPA teaches receiving active thread state of the first active thread (page 3, par. 005, lines 4-7, specification).

14. As per claim 10 and 11, they have similar limitations as of claims 5 and 3 above. Therefore they are rejected under the same rational as of claims 5 and 3 above.

15. As per claim 13, Flynn teaches forwarding the virtual thread state corresponding to the first active thread to state update logic (figure 2, instruction dispatch from the output multiplexer 16).

Flynn does not specifically forwarding the thread state to the state update logic.

However, AAPA teaches receiving active thread state of the first active thread and forwarding the thread state to the state update logic (page 3, par. 005, lines 4-7, specification).

16. As per claim 14, Flynn teaches detecting the activation of the second active thread(col 4, lines 19-24; lines 61-65);

receiving active thread state of the second active thread if the activation of the second active thread is detected(col 4, lines 13-18);

updating the virtual thread state in accordance with the active thread state of the second active thread(col 4, lines 61-65); and

forwarding the virtual thread state corresponding to the second active thread (figure 2, instruction dispatch from the output multiplexer 16).

Flynn does not specifically disclose forwarding the thread state to the state update logic.

However, AAPA teaches forwarding the thread state to the state update logic (page 3, par. 005, lines 4-7, specification).

17. As per claim 15, Flynn teaches the invention substantially as claimed including a processor, comprising:

a virtual state reload multiplexer to receive active thread state of a first active thread(col 4, lines 13-18; figure 2, element 12); and

generate virtual thread state in accordance with the active thread state (col 3, lines 63-67 through col 4, lines 1-18)

Flynn does not specifically disclose a state register to generate thread state in accordance with the active thread state of the first active thread.

However, AAPA teaches a state register to generate thread state in accordance with the active thread state of the first active thread (figure 1, par. 005, lines 1-9)

18. As per claim 16, it has similar limitations as of claim 13 above. Therefore it is rejected under the same rational.

19. As per claim 17, Flynn teaches virtual state reload multiplexer is further to: maintaining the virtual thread state comprising reloading the virtual thread state corresponding to the first active thread until the first active thread becomes inactive and a second active thread becomes active(col 4, lines 13-18; figure 2, element 16); and

receive active thread state of the second active thread if the activation of the second active thread is detected (col 4, lines 13-18).

20. As per claim 18, Flynn teaches detect the activation of the second active thread(col 4, lines 19-24; lines 61-65);

update the virtual thread state corresponding to the second active thread(col 4, lines 61-65); and

forwarding the virtual thread state corresponding to the second active thread (figure 2, instruction dispatch from the output multiplexer 16).

Flynn does not specifically disclose forwarding the thread state to the state update logic.

However, AAPA teaches forwarding the thread state to the state update logic (page 3, par. 005, lines 4-7, specification).

21. As per claims 19-22, they have similar limitations as of claims 15-18 above. Therefore they are rejected under the same rational as of claims 15-18 above.

22. As per claims 23-26, they have similar limitations as of claims 1 and 5-7 above. Therefore they are rejected under the same rational as of claims 1 and 5-7 above.

23. As per claims 28-30, they have similar limitations as of claims 9-10 and 14. Therefore they are rejected under the same rational as of claims 9-10 and 14 above.

24. Claims 4, 8, 12 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flynn et al.(Flynn) US Patent No. 5907702, in view of Applicant Admitted Prior ART(AAPA), and in view of Joy et al.(Joy) US Patent No. 6341347.

25. As per claim 4, Flynn and AAPA do not specifically disclose generating of the virtual thread state is performed by a state register of the virtual state mechanism.

However, Joy teaches generating of the thread state is performed by a state register (col 8, lines 33-39; col 15, lines 1-7).

26. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Joy into the combined method of Flynn and AAPA to use a state register to generate the thread state. The modification would have been obvious because one of the ordinary skills of the art would use a state register to identify the active thread in a multi-threaded system as it is a well known operation in a multi-threaded system to select the active thread from multiple threads.

27. As per claim 8, Joy teaches detecting an uncommon event in a path between the state update logic and the first active thread (col 2, lines 21-28; col 15, lines 8-26) ; and

performing state restoration corresponding to the first active thread (col 15, lines 18-26).

Joy does not specifically disclose using a state restoration multiplexer.

However AAPA teaches using a state restoration multiplexer (figure 1, element 118, 120, 122, 124)

28. As per claim 12, it has similar limitations as of claim 4 above. Therefore it is rejected under the same rational as of claim 4 above.

29. As per claim 28, it has similar limitations as of claim 8 above. Therefore it is rejected under the same rational as of claim 8 above.

Response to Arguments

30. Applicant's arguments filed 12/02/2008 have been fully considered but they are not persuasive.

31. In the remarks applicant argues:

(1) Regarding 112 rejection the claim language rejected by the examiner derives support and clarity from the specifications and figures.

(2) Flynn and AAPA fails to teach "using a virtual state mechanism " and "generating virtual thread state in accordance with the active thread state of the first active thread".

32. Examiner respectfully disagree with applicant:

i. As to point (1), applicant supports his argument mentioning that figure 3 and specification paragraph [0031]-[0040] provides support and clarity of the claim language. In response to applicant's argument it is noted that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. Appropriate correction to provide clarity and precision or concise explanation of how the claimed limitations show the relationship between the elements can be defined such a way that one of ordinary skill in the art is required.

ii. As to point (2), applicant supports his argument mentioning that Flynn and AAPA fails to disclose those limitations as a statement without any analysis or expiation how the limitation fails to disclose the claimed invention. The claimed limitation is broad and does not specify what is a "virtual state mechanism" and how it is being used to receive the active thread state. Examiner interprets the thread switch mechanism in Flynn as the virtual state mechanism that identifies the thread that is becoming active with preparing the instruction needed for the active thread (col 2, lines 57-64). Applicant also argues that Flynn fails to teach "generating the virtual thread state in accordance with the active thread state". The limitations if broad and does not specify what is a **virtual thread state** and where and how it is generated using the active thread state. The examiner interprets

the limitations as generating a virtual thread state by making the thread switch signal low and using the active thread with the instruction fill multiplexer 12 with the received output signal to generate the virtual state (col 4, lines 19-24).

Conclusion

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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